



UNITED STATES PATENT AND TRADEMARK OFFICE

sh
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,461	07/21/2003	Cherng-Chiao Wu	2410-0173P	5230
2292	7590	09/27/2004		EXAMINER
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			WARREN, MATTHEW E	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/622,461	WU
	Examiner	Art Unit
	Matthew E Warren	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 21 July 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-10 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-10 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

Claim 10 is objected to because of the following informalities: the claim contains the limitation of "the lower unit" and "the cavity of the surface of the printed circuit board." There is insufficient antecedent basis for the limitations in the claims. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Chun (US 6,407,448 B2).

In re claim 1, Chun shows (fig. 3-5A) a stacking apparatus for integrated circuit assemblies comprising at least one substrate (25) and one integrated circuit assembly (1, 2, 3, 4, and 5) stacking over each other, wherein the substrate has an opening in the center of a upper surface of the substrate and a plurality of solder spots (near 4c) located on the periphery of the opening, the solder spots being electrically connected to a lower surface (27) of the substrate; and the integrated circuit assembly sunk in the aforementioned opening, with its legs (4c) soldering on the solder spots of the

substrate, combining the substrate to make a unit structure; two or more such units (110, 110, etc.) can be stacked and soldered over each other, with their bottom soldering to a surface of a printed circuit board (col. 3, lines 52-58).

In re claims 3, 5, 6, 8, and 9, Chun shows (fig. 3-5A) that the opening in the center of the substrate is a cavity sunk from the surface of the substrate. The periphery of the cavity has solder spots (4c) that are electrically connected to the other surface of the substrate through via (26) and connected to the printed circuit board through balls (8). The units are soldered and coupled through corresponding legs (108a) located on an upper layer unit (110) and a lower layer unit (100), the substrate of the lower layer unit has a bottom side with legs (8b in fig. 5H) bonding to the printed circuit board (by balls 8) to form stacking.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chun (US 6,407,448 B2) as applied to claim 1 above, and further in view of Farnworth et al. (US 6,020,629).

In re claims 2 and 4, Chun shows all of the elements of the claims except the opening in the center of the substrate being a through hole. Farnworth et al. shows (figs. 1-2D) a semiconductor stacking apparatus having a substrate (22) with an opening being a through hole formed through the upper and lower surface of the substrate. With this configuration a semiconductor integrated circuit assembly can be formed in the substrate and configured to provide a planar surface to further facilitate stacking of the substrates (col. 2, lines 10-25). Farnworth also shows that the periphery of the cavity has solder spots (42RF) that are electrically connected to the other surface of the substrate through via (44) and connected to the printed circuit board through balls (42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the substrate of Chun by forming the opening as a through hole as taught by Farnworth to form a planar IC assembly that would better facilitate stacking of subsequent stacking apparatuses.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chun (US 6,407,448 B2) as applied to claim 1 above, and further in view of Brandenburg et al. (US 2004/0113281 A1).

In re claim 7, Chun shows all of the elements of the claims except the air vents communicating with the opening in the center. Brandenburg et al. discloses [0022] that air vents in a package allows unwanted air to escape the package during a subsequent molding process. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the substrate of Chun by forming air vents

Art Unit: 2815

in the substrate as taught by Brandenburg to allow unwanted air or gas to escape the assembly during the molding or packaging process.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chun (US 6,407,448 B2) as applied to claim 1 above, and further in view of Harada et al. (US 2001/0054481 A1).

In re claim 10, Chun shows all of the elements of the claims except the bottom of a lower unit sinking into a cavity of the surface of the printed circuit board. Harada et al. discloses [0006-0007] that a cavity may be formed in a circuit board and have devices mounted therein to reduce the thickness of a multi-layered circuit board and ultimately reduce the size of an electronic device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the printed circuit board of Chun by forming a cavity within it as taught by Harada to form assemblies within the cavity and ultimately reduce the size of the electronic device.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Glenn (US 6,746,476 B1) also shows a stackable assembly that has legs for connecting to a circuit board.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E Warren whose telephone number is (571)

Art Unit: 2815

272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
MEW
September 23, 2004

Tom Thomas
TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800